AMENDMENTS TO THE CLAIMS

The following is a complete listing of revised claims with a status identifier in parenthesis.

LISTING OF CLAIMS

1. (Currently Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an output signal;

a gain control unit having a dual feedback loop for gain control and responding to the self bias signal and the output signal.

2. (Original) The input buffer circuit of claim 1, wherein the gain control unit comprises:

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal.

3. (Original) The input buffer circuit according to claim 2, wherein the gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal; and

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

4. (Currently Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an output signal;

a gain control unit having a dual feedback loop for gain control responsive to the self bias signal and the output signal; and

a current controlling circuit that supplies current to the first inverting switch, the second inverting switch and the gain control unit and sinks current from the first inverting switch, the second inverting switch and the gain control unit, the current controlling circuit responding to the self bias signal.

5. (Original) The input buffer circuit of claim 4, wherein the gain control unit comprises:

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal.

6. (Previously Amended) The input buffer circuit according to claim 5, wherein the gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal;

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

7. (Previously Amended) The input buffer circuit of claim 5, wherein the current controlling circuit comprises:

a third PMOS transistor having a source connected to the first node, a drain connected to the gain control unit to supply current and a gate connected to the self bias signal; and

a third NMOS transistor having a source connected to the second node, a drain connected to the gain control unit to sink current and a gate connected to the self bias signal.

8. (Currently Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an output signal;

a gain control unit having a dual feedback loop for gain control responsive to the self bias signal and the output signal; and

a swing width control circuit connected to a feedback signal that is inverted by the output signal.

9. (Original) The input buffer circuit of claim 8, wherein the gain control unit comprises:

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal.

10. (Original) The input buffer circuit of claim 9, wherein the gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal;

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

11. (Previously Amended) The input buffer of claim 8, wherein the swing width control circuit comprises:

an NMOS transistor having a source connected to the gain control unit, a drain connected to the gain control unit and a gate connected to the feedback signal; and

a PMOS transistor having a source connected to the output signal, a drain connected to the gain control unit and a gate connected to the feedback signal.

12. (Currently Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an output signal;

a gain control unit having a dual feedback loop for gain control responsive to the self bias signal and the output signal;

a current controlling circuit that supplies current to the first inverting switch, the second inverting switch and the gain control unit and sinks current from the first inverting switch, the second inverting switch and the gain control unit, the current controlling circuit responding to the self bias signal; and

a swing width control circuit connected to a feedback signal that is inverted by the output signal.

13. (New) The input buffer circuit of claim 1, wherein the dual feedback loop includes a first feedback loop including at least one node and at least one PMOS transistor and a second feedback loop including at least one node and at least one NMOS transistor.

14. (New) The input buffer circuit of claim 13, wherein the first feedback loop, the self bias signal is supplied to a first node, a gate of a first PMOS transistor, a gate of a second PMOS transistor, a second node, a source of a third PMOS transistor and back to the first node to complete the first feedback loop.

15. (New) The input buffer of claim 13, wherein the second feedback loop, the self bias signal is supplied to a first node, a gate of a first NMOS transistor, a gate of a second NMOS transistor, a source of a third NMOS transistor and back to the first node to complete the second feedback loop.

16. (New) The input buffer circuit of claim 4, wherein the dual feedback loop includes a first feedback loop including at least one node and at least one PMOS transistor and a second feedback loop including at least one node and at least one NMOS transistor.

17. (New) The input buffer circuit of claim 16, wherein the first feedback loop, the self bias signal is supplied to a first node, a gate of a first PMOS transistor, a gate of a second PMOS transistor, a second node, a source of a third PMOS transistor and back to the first node to complete the first feedback loop.

18. (New) The input buffer of claim 16, wherein the second feedback loop, the self bias signal is supplied to a first node, a gate of a first NMOS transistor, a gate of a second NMOS transistor, a source of a third NMOS transistor and back to the first node to complete the second feedback loop.

19. (New) The input buffer circuit of claim 8, wherein the dual feedback loop includes a first feedback loop including at least one node and at least one PMOS transistor and a second feedback loop including at least one node and at least one NMOS transistor.

20. (New) The input buffer circuit of claim 19, wherein the first feedback loop, the self bias signal is supplied to a first node, a gate of a first PMOS transistor, a gate of a second PMOS transistor, a second node, a source of a third PMOS transistor and back to the first node to complete the first feedback loop.

21. (New) The input buffer of claim 19, wherein the second feedback loop, the self bias signal is supplied to a first node, a gate of a first NMOS transistor, a gate of a second NMOS transistor, a source of a third NMOS transistor and back to the first node to complete the second feedback loop.

22. (New) The input buffer circuit of claim 12, wherein the dual feedback loop includes a first feedback loop including at least one node and at

least one PMOS transistor and a second feedback loop including at least one node and at least one NMOS transistor.

23. (New) The input buffer circuit of claim 22, wherein the first feedback loop, the self bias signal is supplied to a first node, a gate of a first PMOS transistor, a gate of a second PMOS transistor, a second node, a source of a third PMOS transistor and back to the first node to complete the first feedback loop.

24. (New) The input buffer of claim 22, wherein the second feedback loop, the self bias signal is supplied to a first node, a gate of a first NMOS transistor, a gate of a second NMOS transistor, a source of a third NMOS transistor and back to the first node to complete the second feedback loop.